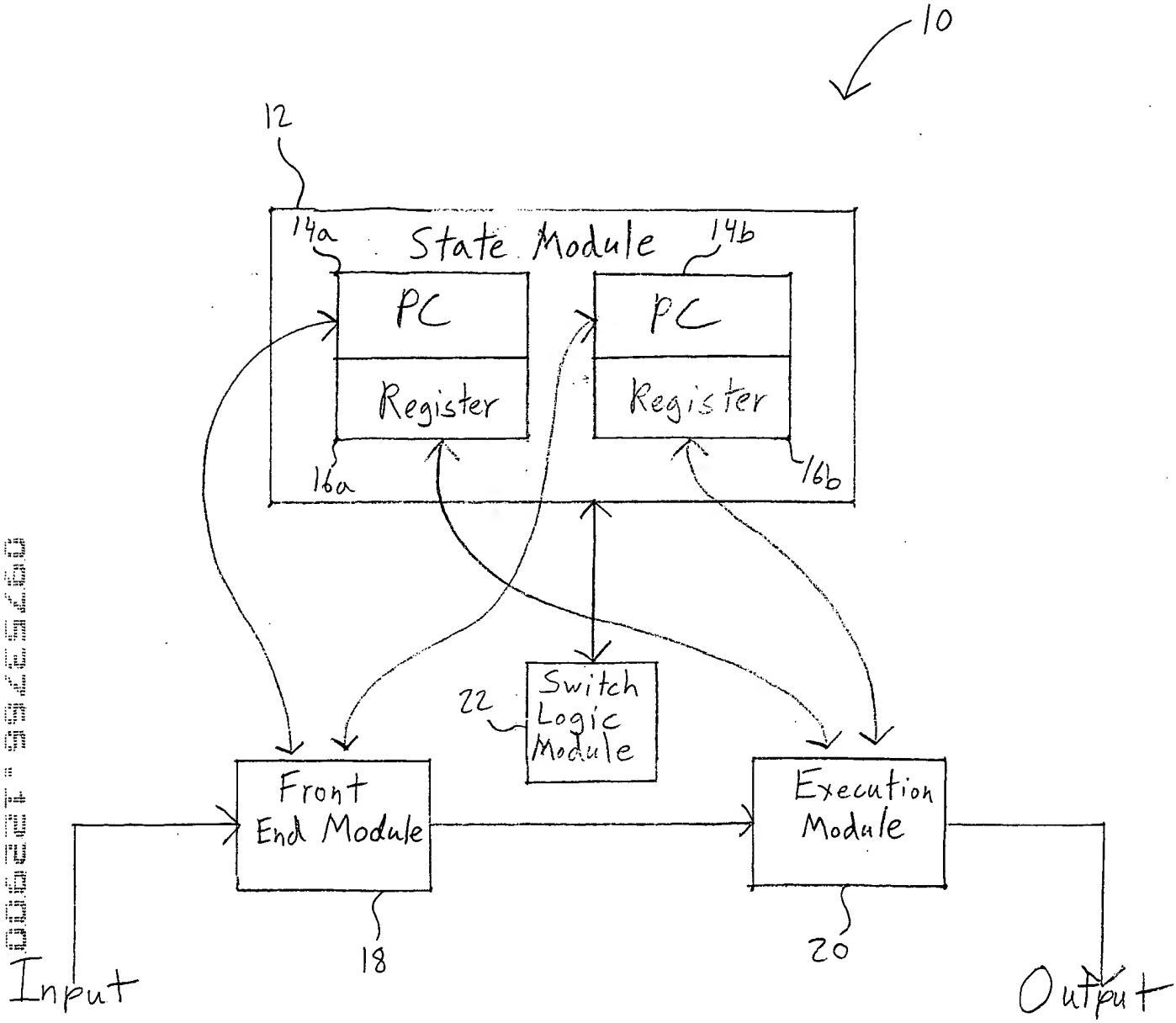
10
12
14a
State Module
14b
PC
Register
PC
Register
16a
16b
22
Switch Logic Module
Front End Module
Execution Module
18
20
Input
Output

Fig. 1

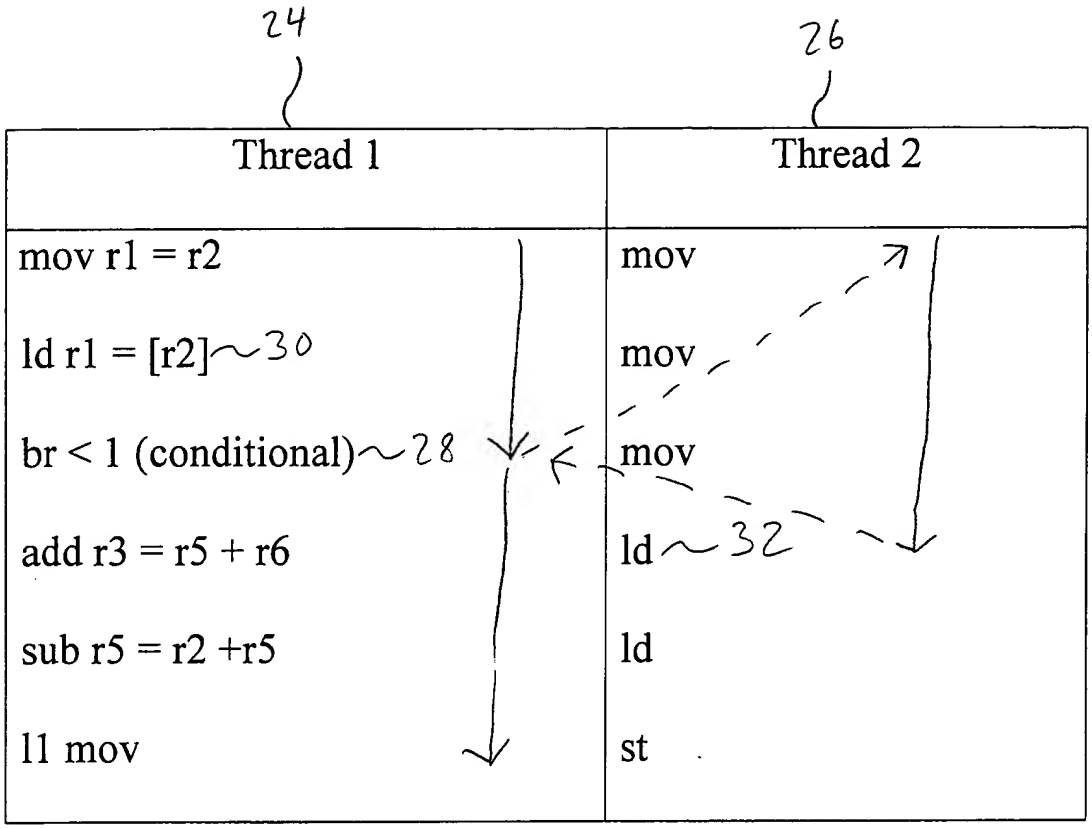
24
26
Thread 1
Thread 2
mov r1 = r2
ld r1 = [r2]
30
br < 1 (conditional)
28
add r3 = r5 + r6
sub r5 = r2 +r5
l1 mov
mov
mov
mov
ld
32
ld
st

Fig. 2

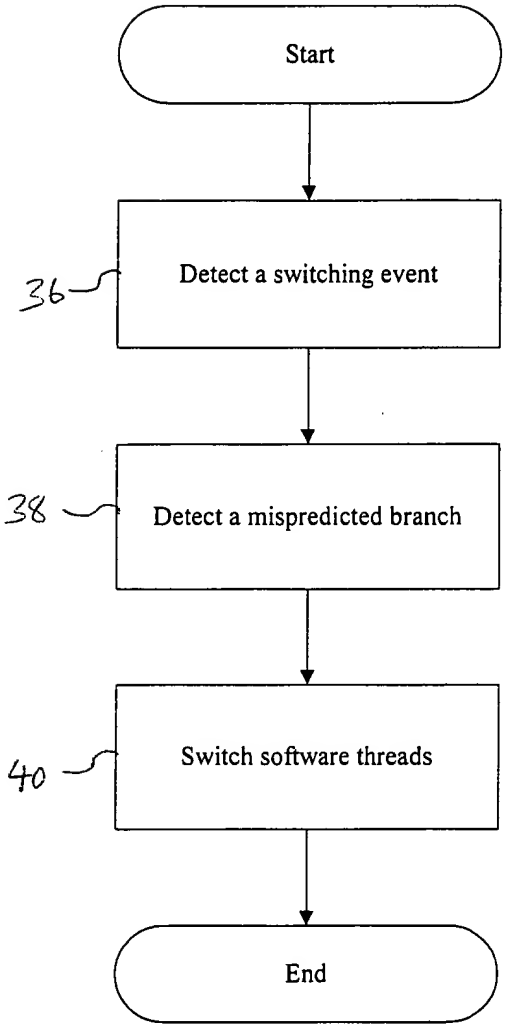
34
Start
36
Detect a switching event
38
Detect a mispredicted branch
40
Switch software threads
End

Fig. 3

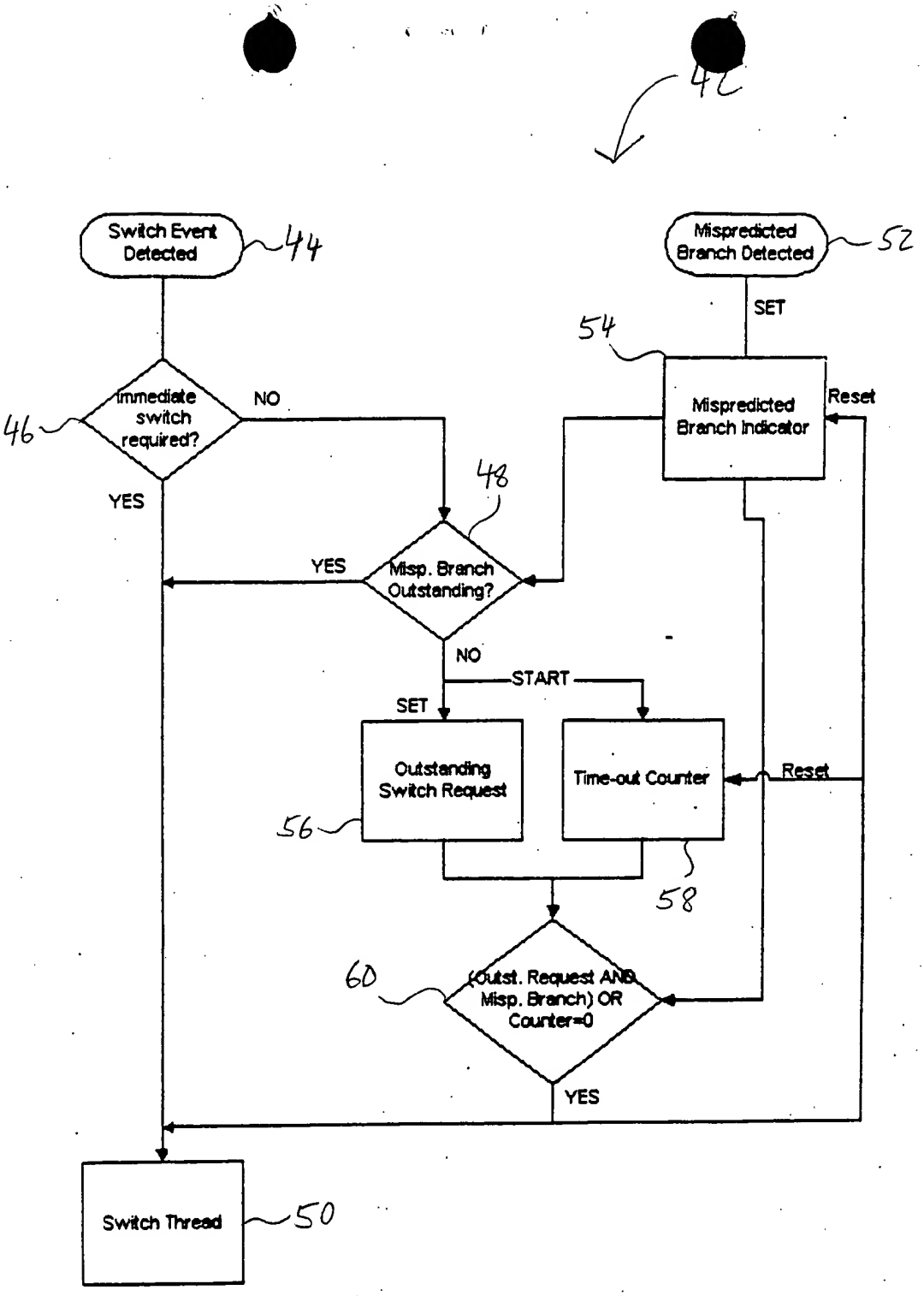
42
Switch Event Detected
44
Mispredicted Branch Detected
52
SET
54
Mispredicted Branch Indicator
Reset
Immediate switch required?
46
NO
YES
48
Misp. Branch Outstanding?
YES
NO
START
SET
Outstanding Switch Request
56
Time-out Counter
Reset
58
(Outst. Request AND Misp. Branch) OR Counter=0
60
YES
Switch Thread
50

Fig. 4